We claim:

1. **A method** for hermetically sealing of dielectrically insulating isolation trenches by filling with a deposition method, wherein the trenches (1, 2) are slightly broadened at specific positions (2) and a low pressure deposition technique is used such that void channels (5) forming in the area of the trenches having normal width by closing the upper trench portions with a fill material (9) are hermetically sealed in the longitudinal direction of the trench by means of low pressure material deposition from the broadened trench portion (2, 3) along the length direction of the trench.

2. The method of claim 1, wherein the broadened trench positions (2, 3) in the vicinity of the bond surfaces of the two semiconductor wafers during the bonding of the two wafers are provided more densely than along the other parts of the isolation trenches.

3. The method of claim 1, wherein the broadened trench positions (2, 3) are provided in regular intervals.

4. **An assembly** manufactured or manufacturable according to one of the aforementioned methods.

5. **A method** for hermetically sealing dielectrically insulating isolation trenches (trenches 1, 2) by filling with a deposition technique,
   (i) wherein the isolation trenches (1, 2) are slightly broadened (2, 3) at at least one specific position;
   (ii) a low pressure deposition technique is used to hermetically seal a void (5) in a longitudinal direction of the isolation trench by means of a low pressure material deposition starting from the broadened trench portion (2, 3) along the length direction of the trench, wherein said void is formed in the area of the isolation trenches (1) having the normal width due to the closure of upper trench portions with fill material (9).

6. The method of claim 5, wherein the broadened trench positions (2) are provided in the vicinity of the bonding surfaces of two semiconductor wafers more densely than along the other sections of the isolation trenches during bonding of the wafers.

7. The method of claim 5, wherein a plurality of broadened trench positions (2) are provided in regular intervals for forming sealing positions along a channel (1, 2, 1).

8. The method of claim 5, wherein the slightly broadened isolation trenches (1, 2) are broadened at the at least one position according to a width that is not greater than the width of the trench (1) at the non-broadened position.

9. The method of claim 8 or 5, wherein the broadening (2, 3) is provided by conical sections (3).

10. The method of claim 5, wherein the low pressure technique is performed substantially at vacuum conditions.

11. The method of claim 5, wherein the broadening (2, 3) is provided at at least a short piece compared to the total length of the channel.

12. The method of claim 5, wherein the selection of parameters of the deposition process and of a trench configuration is performed such that possibly remaining lateral voids (5) are completely sealed before the trench section having the slight broadening (b2) closes in the upwards direction so that a further filling cannot take place.

13. A device comprising a wafer having formed therein isolation trenches, said wafer including hermetically sealed dielectrically insulating isolation trenches (trenches 1, 2) formed by filling with a deposition method,

(i) wherein the isolation trenches (1, 2) are slightly broadened (2, 3) at at least one specific position;

(ii) wherein void channels (5) are hermetically sealed (7) in the longitudinal direction of the trench by a low pressure material deposition from the broadened trench portion (2, 3) in the longitudinal direction of the trench filled by means of a low pressure deposition technique, said void channels being formed during the filling in the area of the trenches (1) having the normal width by closing the upper trench portions with fill material.

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